SPEECH SYNTHESIZER

FIELD OF THE INVENTION

The present invention relates generally to a speech synthesizer, and more particularly, to a speech synthesizer operated in a low frequency with a push-pull drive.

BACKGROUND OF THE INVENTION

For consumer electronic products, it is an important function of digital sound effects, which is outputted on speakers typically by two methods, digital-to-analog converter (DAC) drive method and push-pull drive method such as pulse width modulation (PWM).

Fig. 1 shows the block diagram of a conventional DAC speech synthesizer 100 which includes three basic units, volume control unit 101, signal transform unit 102 and drive unit 103. The volume control unit 101 receives a control signal Vctrl and then generates a control bias Vbias, the signal transform unit 102 receives the control bias Vbias and PCM codes to transform into an analog speech signal Ivo, and the drive unit 103 receives the analog

speech signal Ivo and amplifies it to be a current Ispeaker to drive a speaker 104. Fig. 2A is the waveform of a 7-bits sinusoidal PCM signal, Fig. 2B is the waveform of the analog speech signal Ivo after the PCM signal shown in Fig. 2A is processed by the signal transform unit 102 shown is Fig. 1, and the waveform of the output current signal Ispeaker after the analog speech signal Ivo is amplified by the drive unit 103 is shown in Fig. 2C. As shown in Fig. 2C, when a conventional DAC speech synthesizer transforms a digital speech signal back to an analog signal, the current signal Ispeaker has a zero point about 300 mA, which leads to a more power consumption as shown in the area with dashed lines in Fig. 2C. For applications of portable electronic products whose power supply is battery, such large power consumption should be avoided. Moreover, to prevent the transistor 105 within the drive unit 103 from saturated to result in a speech distortion, a bypass resistor 106 is inserted thereof, which further results in the speech distortion more seriously.

Shown in Fig. 3 is a push-pull output circuit diagram of a PWM speech synthesizer, which improves the power consumption and needs no additional transistors employed in the speech synthesizer. Fig. 4A is the waveform of a 7-bits sinusoidal PCM signal, Fig. 4B shows the modulated signals SPK1 and SPK2 respectively corresponding to the positive and negative half cycles of the PCM signal shown in Fig. 4A after processed by the push-pull

speech synthesizer shown in Fig. 3, and the waveform of the output current signal Ispeaker for the speaker transformed from the PWM modulated signals SPK1 and SPK2 is shown in Fig. 4C.

To drive a PWM speech synthesizer, there is necessary to provide an operation frequency

$$f = fs \times 2n\text{-}1 \times m,$$

[Eq-1]

where fs is sampling frequency, n is bit numbers of PCM data, and m is output pulse number for each sample. 2n-1 in Eq-1 represents the resolution of the speech signal. When a desired resolution or output pulse number is increased, the operation frequency is also increased. If more than one sampling frequency are available for a synthesizer, the operation frequency has to be a common multiple of the sampling frequencies and is thus generally high.

SUMMARY OF THE INVENTION

To resolve the above problems, the present invention is therefore directed to a speech synthesizer with reduced power consumption and operation frequency.

According to the present invention, a speech synthesizer comprises a signal transform unit to receive and transform a series of digital speech codes to be an analog speech signal with the most significant bit (MSB) of each digital speech code to control the transformation of the digital speech codes, and a current output unit connected to the signal transform unit, which includes a first and second signal output terminals and receives the analog speech signal with the MSB of each digital speech code to control the current output direction of the current output unit.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be had to the following description of exemplary embodiments thereof, considered in conjunction with the accompanying drawings, in which:

Fig. 1 shows the block diagram of a conventional DAC speech synthesizer;

Fig. 2A is the waveform of a 7-bits sinusoidal PCM signal;

Fig. 2B is the waveform of the analog speech signal Ivo after the PCM signal shown in Fig. 2A is processed by the signal

transform unit 102 shown is Fig. 1;

Fig. 2C is the waveform of the output current signal Ispeaker after the analog speech signal Ivo shown in Fig. 2B is amplified by the drive unit 103;

Fig. 3 is a push-pull output circuit diagram of a PWM speech synthesizer;

Fig. 4A is the waveform of a 7-bits sinusoidal PCM signal;

Fig. 4B is the modulated signals SPK1 and SPK2 respectively corresponding to the positive and negative half cycles of the PCM signal shown in Fig. 4A after processed by the push-pull speech synthesizer shown in Fig. 3;

Fig. 4C is the waveform of the output current signal Ispeaker for the speaker transformed from the PWM modulated signals SPK1 and SPK2;

Fig. 5 is the block diagram of a preferred embodiment speech synthesizer according to the present invention;

Fig. 6 is an implemented circuit diagram of the signal transform unit within the speech synthesizer shown in Fig. 5;

Fig. 7A is a 7-bits sinusoidal PCM digital speech signal;

Fig. 7B is the output signal from the signal transform unit after the PCM signal shown in Fig. 7A is processed by the speech synthesizer shown in Fig. 5;

Fig. 8A is the first type connection of the current output unit and speaker for the speech synthesizer of the present invention;

Fig. 8B is the second type connection of the current output unit and speaker for the speech synthesizer of the present invention;

Fig. 8C is the third type connection of the current output unit and speaker for the speech synthesizer of the present invention;

Fig. 9 is a detailed circuit for the current output unit shown in Fig. 8A; and

Fig. 10 is the waveform of the drive current generated by the current output unit shown in Fig. 9 from the analog speech signal shown in Fig. 7B.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 5 shows the block diagram of a preferred embodiment speech synthesizer according to the present invention. As shown in this figure, a speech synthesizer 50 comprises three basic units, volume control unit 51, signal transform unit 52 and current output unit 53, in which the volume control unit 51 receives a control signal Vctrl and generates a control bias Vbias transmitted to the signal transform unit 52 to adjust the volume with a function similar to that of the volume control unit 101 within the conventional DAC speech synthesizer 100.

Fig. 6 shows an implemented circuit diagram of the signal transform unit 52, which receives the control bias Vbias and a series of digital speech signal D [0:6], and then transforms into an analog speech signal Ivo. As shown in the figure, the signal transform unit 52 includes a switched buffer 521 and a switched inverter buffer 522 connected in parallel, and a DAC 523. The switched buffer 521 and inverter buffer 522 receive the lower bits data D [5:0] of the PCM digital speech signal under the control of the MSB D6 in a manner that the switched buffer 521 is enabled to transfer the lower bits data D [5:0] to the DAC 523 when MSB=1 and the switched inverter buffer 522 is enabled to transfer the inverse of the lower bits data D [5:0] to the DAC 523 when MSB=0. The DAC 523 transforms the lower bits data D [5:0] transmitted from the switched buffer 521 and

inverter buffer 522 into the analog speech signal Ivo. As shown in Fig. 7A, a 7-bits sinusoidal PCM digital speech signal has a zero position of 40H, and thus the MSBs of whose upper and lower half cycles are 1 and 0 respectively. The PCM digital speech signal is therefore transformed by the signal transform unit 52 into the analog speech signal Ivo shown in Fig. 7B.

The controls of the current output unit 53 for different type connections are illustrated in Fig. 8. Based on the push-pull operation, the current output unit 53 outputs a current in different directions corresponding to positive and negative half cycles to directly drive a speaker. As shown in the figure, the current output unit 53 includes a first control switch 701, a second control switch 702, a first switched current source 703 and a second switched current source 704, all of them are under controlled by the MSB of the digital speech signal, and a first current output terminal V01 and a second current output terminal V02 to output the drive current to the connected speaker 54. There are two types for the output current of the current output unit 53. In detail, when MSB=1, the first control switch 701 and first switched current source 703 are conducted so as for the drive current to flow from the first current output terminal V01 to the second current output terminal V02 through the speaker 54, and the second control switch 702 and second switched current source 704 are conducted so as for the drive current to flow from the second current output terminal

V02 to the first current output terminal V01 through the speaker 54 when MSB=0. This way the current output unit 53 generates a push-pull output current to drive the speaker 54.

The first type connection for the current output unit 53 is shown in Fig. 8A, in which the first control switch 701 is connected to a power supply VDD with one end and the second switched current source 704 with the other that is also the first current output terminal V01, and the other end of the second switched current source 704 is connected to a low voltage such as grounded. On the other hand, the second control switch 702 is connected to a power supply VDD with one end and the first switched current source 703 with the other that is also the second current output terminal V02, and the other end of the first switched current source 703 is connected to a low voltage such as grounded.

The second type connection for the current output unit 53 is shown in Fig. 8B, in which the first switched current source 703 is connected to a power supply VDD with one end and the second switched current source 704 with the other that is also the first current output terminal V01, and the other end of the second switched current source 704 is connected to a low voltage such as grounded. On the other hand, the second control switch 702 is connected to a power supply VDD with one end and the first control switch 701 with the other that is also the second current output

terminal V02, and the other end of the first control switch 701 is connected to a low voltage such as grounded.

The third type connection for the current output unit 53 is shown in Fig. 8C, in which the first switched current source 703 is connected to a power supply VDD with one end and the second control switch 702 with the other that is also the first current output terminal V01, and the other end of the second control switch 702 is connected to a low voltage such as grounded. On the other hand, the second switched current source 704 is connected to a power supply VDD with one end and the first control switch 701 with the other that is also the second current output terminal V02, and the other end of the first control switch 701 is connected to a low voltage such as grounded.

A detailed circuit for the current output unit 53 shown in Fig. 8A is provided in Fig. 9, and the circuits for those shown in Figs. 8B and 8C can be easily obtained in reference to the correspondence between Fig. 9 and Fig. 8A. The current output unit 53 in Fig. 9 includes a first transistor 906 serving as the first control switch 701, a second transistor 907 serving as the second control switch 702, a first variable current controlled switch 905 to control the first switched current source 703 and a second variable current controlled switch 904 to control the second switched current source 704. The current output unit 53 further includes a third transistor

903 and fourth transistor 909 to form a current mirror for the first switched current source 703 and a fifth transistor 908 in combination with the third transistor 903 to form another current mirror for the second switched current source 704.

For the circuit shown in Fig. 9, when the MSB of the digital speech signal is 1, the first transistor 906 and the first variable current controlled switch 905 are conducted so as for the drive current to flow through a current path that is formed from the first transistor 906 to the fourth transistor 909 through the first current output terminal V01, speakers 54 and second current output terminal V02 with its magnitude controlled by the Ivo and current mirror composed of the third and fourth transistors 903 and 909. On the contrary, when the MSB of the digital speech signal is 0, the second transistor 907 and the second variable current controlled switch 904 are conducted so as for the drive current to flow through another current path that is formed from the second transistor 907 to the fifth transistor 908 through the second current output terminal V02, speakers 54 and first current output terminal V01 with its magnitude controlled by the Ivo and current mirror composed of the third and fifth transistors 903 and 908. As a result, the current passing through the speaker 54 has a zero position of 0 mA as shown in Fig. 10, there is thus no additional DC current consumption induced.

From the above, it should be understood that the embodiments described, in regard to the drawings, are merely exemplary and that a person skilled in the art may make variations and modifications to the shown embodiments without departing from the spirit and scope of the present invention. All variations and modifications are intended to be included within the scope of the present invention as defined in the appended claims.